# A Closed-Loop Using Sampled-Data Controller for a New Nonisolated High-Gain DC–DC Converter

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***Abstract*—This article tries closed-loop using a sampled-data (SD) controller for a new nonisolated dc–dc converter to maintain the constant voltage. The developed nonisolated converter attains a higher voltage gain and reduced voltage stress across the power semiconductor switch. The converter topology provides a higher voltage gain (10) at a duty ratio of 0.6. The operation of the proposed converter is discussed in continuous conduction mode, discontinuous conduction mode, and boundary conduction mode. The performance of the converter is examined under open-loop and closed-loop conditions by changing the duty ratio and load values. An SD control increases the control performance in the closed-loop condition. The suggested Lyapunov functional can entirely use system data. Exponential stability criteria created by linear matrix inequalities are deduced using improved inequality techniques and some sufficient conditions. Average dwell time is calculated as a type of inequality considering the sample interval. A laboratory-based experimental prototype is designed to corroborate the performance of the proposed converter in open-loop and closed-loop operations during steady-state and dynamic conditions. The effectiveness of the developed converter is analyzed by comparing the voltage gain, the ratio of voltage stress to voltage gain, and the ratio of voltage gain to total component count with recently developed quadratic-based converters and nonquadratic-based converters. A component stress factor and switch device power are examined to showcase the voltage stress and power handling capability. Experimental results are closely matched with the theoretical calculations. The power density of the proposed converter is 1.02 kW/L.**

***Index Terms*—Converter, dynamic condition, sampled-data control (SDC), voltage gain.**

## I. Introduction

A HIGH-GAIN dc–dc converter is essential in a photovoltaic (PV) system for enhanced energy harvesting, increased system efficiency, extended operating range, grid integration, and system flexibility [1]. It plays a significant role in optimizing the performance and reliability of the PV system, meeting the requirements of the loads or grid [1]. Isolated and nonisolated converters are the two major classifications where nonisolated converters are preferred over isolated converters to avoid core losses, more weight, space, and high cost [2], [3]. In the last two decades, many nonisolated converters have been proposed in the literature. Still, many researchers focus on creating a new nonisolated converter to improve performance, efficiency, reliability, and cost-effectiveness. Quadratic boost converter (QBC) is a nonisolated converter category that yields a higher voltage gain at a lower duty ratio than the conventional converter categories [4].

The developed QBC topologies in the existing literature have been created either by combining two different conventional converter topologies in [5], [6], [7], [8] or the addition of voltage multiplier cells (VMCs) with basic QBC in [9], [10], [11], and [12] or the addition of passive components in the primary conventional converters to perform a quadratic nature operation in [13], [14], [15], [16], and [17]. The converter in [7] has been developed by combining the QBC with the Cuk converter to attain a higher voltage gain. Still, the power loss of the developed converter is high, which may reduce the efficiency of the converter. The converter in [8] has utilized two semiconductor switches which may increase the power loss and size of the converter. The converter in [9] has utilized a single VMC cell to attain a higher voltage gain, but the voltage stress of the switch is high (i.e., an output voltage of the converter), which reduces the lifetime of the devices. The converter in [10] has been developed with a single VMC cell, but it contains two semiconductor switches, which may increase the converter's size and control complexity. The developed converter in [11] and [12] has utilized VMC with a single switch. However, the voltage stress of the power semiconductor switch is equal to the output voltage of the converter. The converter developed in [12] is operated at a higher switching frequency (100 kHz), which may increase the switching loss, output capacitance loss of the switch, and reverse recovery loss of diodes. Also, it utilizes more components, which may increase the overall size of the converter. The developed converter in [13], [14], [15], and [17] has utilized two semiconductor switches which may decrease the overall efficiency by increasing the power loss due to switching and coss losses. Further, it increases the control complexity for a closed-loop operation. The developed converter in [16] has

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attempted to relocate the components concerning the basic QBC, but it cannot provide a higher voltage gain at a less-duty ratio.

Furthermore, a switched system is typically made up of a group of subsystems that operate in continuous or discrete time and a logic rule that is responsible for coordinating the switching between these subsystems [18], [19], [20]. As a class of hybrid systems, switched systems are often used to represent some practical hybrid processes that can hardly be described by continuous or discrete models. Because of these benefits, switched systems have found widespread application in a variety of contexts, including networked control systems, the aerospace industry, and power electronics [21], [22], [23], [24]. Over the course of the previous two decades, several research has been conducted on switched systems in [18], [19], [20], [21], [22], [23], [24], [25], and [26]. As a result of advancements made in communication networks and high-speed digital equipment, digital control is now widely used in many different types of modern industrial control. The digital controller that makes use of the data collected at sampling instants makes it possible for the controlled system to remain steady. When compared to the continuous control, the sampled-data control (SDC) has the potential to significantly enhance the efficacy as well as the economy of the network bandwidth [23], [24], [25], [26].

Most of the QBC topologies in the existing literature suffer from higher voltage stress across the semiconductor devices and the closed-loop control strategies have not been discussed. Therefore, this article attempts to design a new converter under the nonisolated QBC category to attain a higher voltage gain at a lower duty ratio with reduced voltage stress across the semiconductor switch. Also, an SDC strategy is implemented to examine the operating performance of the proposed converter. The unique features of this work are given below.

1) A new nonisolated converter is designed to provide a higher voltage gain (10) at a lower duty ratio (0.6) under the category of the QBC topologies.
2) The ratio of voltage stress to voltage gain ($V_{\mathrm{SW}}/G_{\mathrm{CCM}}$) of the proposed converter is 0.63.
3) The ratio of voltage gain to total component count (TCC) ($G_{\mathrm{CCM}}$/TCC) is 0.83, which indicates the better utilization of components to attain higher voltage gain.
4) The power density of the proposed converter is 1.02 kW/L.
5) The proposed converter operation is examined in steady-state and dynamic conditions by changing duty ratio and load values.
6) The closed-loop condition is implemented with an SDC to examine the proposed converter performance.

## II. Proposed High Gain DC–DC Converter

The proposed nonisolated high gain dc–dc converter topology is shown in Fig. 1(a). It consists of four diodes ($D_1, D_2, D_3, D_4$), three inductors ($L_1, L_2, L_3$), four capacitors ($C_1, C_2, C_3, C_4$), and one switch $M_1$. Continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are explained for the proposed topology. The following assumptions are made to analyze the proposed converter's steady-state equation; all passive semiconductor devices are ideal, and passive elements are large

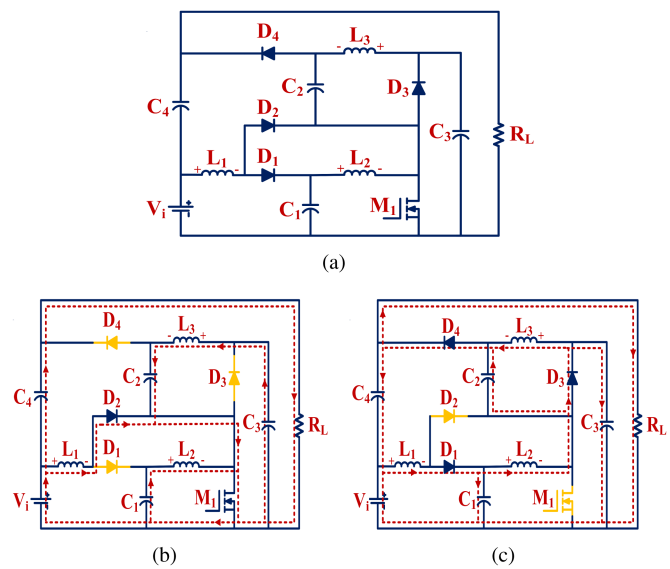



Fig. 1. Proposed converter. (a) Configuration. (b) Mode-I. (c) Mode-II.

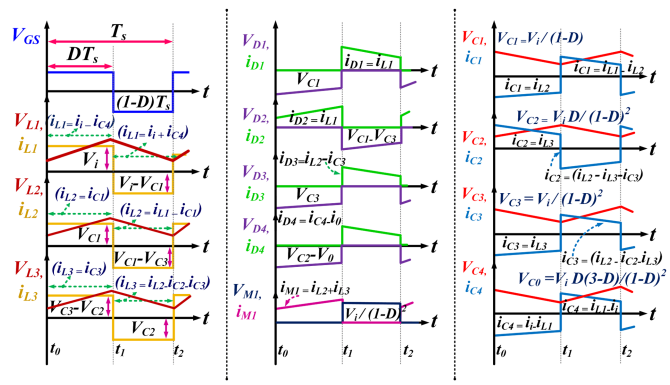



Fig. 2. Theoretical waveform of the proposed converter in CCM.

enough and time-invariant. The current traversal path of the proposed topology for Mode-I and Mode-II in CCM are shown in Fig. 1(b) and 1(c). The theoretical waveform of the proposed converter in CCM is shown in Fig. 2.

### A. Continuous Conduction Mode

*1) Mode-I:* During this mode of operation, the switch $M_1$ is turned ON for time $(0 \leq t \leq t_1)$. So, the inductor $L_1$ is charged by input source $V_i$ through diode $D_2$ and the semiconductor switch $M_1$. The inductor $L_2$ is charged by the capacitor $C_1$ so that the diode $D_1$ is reversed biased. Capacitor $C_3$ is discharged to charge the inductor $L_3$ and capacitor $C_2$ so that the diodes $D_3$ & $D_4$ are reversed biased. The stored energy from the capacitor $C_4$ and input source $V_i$ delivers the power to load $R_L$. Fig. 1(b) shows the current traversal path of the proposed topology. Differential equations derived from Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) are given follows:

$$L_1 \frac{di_{L1}}{dt} = V_i; L_2 \frac{di_{L2}}{dt} = V_{C1}; L_3 \frac{di_{L3}}{dt} = V_{C3} - V_{C2} \quad (1)$$

$$C_1\frac{dv_{C1}}{dt} = -i_{L2}; C_2\frac{dv_{C2}}{dt} = i_{L3} \tag{2}$$

$$C_3\frac{dv_{C3}}{dt} = -i_{L3}; C_4\frac{dv_{C4}}{dt} = -\frac{V_0}{R}. \tag{3}$$

*2) Mode-II:* During this mode of operation, the switch $M_1$ is turned OFF for time $(t_1 \le t \le T_s)$. The capacitor $C_1$ is charged by the input source $V_i$ and inductor $L_1$ through diode $D_1$. The capacitor $C_2$ and inductor $L_3$ discharge their stored energy to charge the capacitor $C_4$ and supply power to load through diode $D_4$. The inductors $L_1$ and $L_2$ discharge their stored energy to charge capacitor $C_3$ through diode $D_3$. Here, the diode $D_2$ is reverse biased. Fig. 1(c) illustrates the current traversal path of the proposed converter in this mode. Differential equations derived from KVL and KCL are given follows:

$$L_1\frac{di_{L1}}{dt} = V_i - V_{C1}; L_2\frac{di_{L2}}{dt} = V_{C1} - V_{C3} \tag{4}$$

$$L_3\frac{di_{L3}}{dt} = V_{C3} - V_0 \tag{5}$$

$$C_1\frac{dv_{C1}}{dt} = i_{L1} - i_{L2}; C_2\frac{dv_{C2}}{dt} = -\left(i_0 + i_{C4} - i_{L3}\right) \tag{6}$$

$$C_3\frac{dv_{C3}}{dt} = i_{L2} + i_{C2} - i_{L3}; C_4\frac{dv_{C4}}{dt} = i_{L3} - i_{C2} - \frac{V_0}{R}. \tag{7}$$

*3) Determination of Voltage Conversion Ratio:* Applying the Volt–Sec balance principle in inductors

$$V_{C1} = \frac{V_i}{1-D}; V_{C3} = \frac{V_{C1}}{1-D} = \frac{V_i}{(1-D)^2} \tag{8}$$

$$V_{C2} = \frac{DV_i}{(1-D)^2}; V_{C4} = \frac{V_i D\,(3-D)}{(1-D)^2}. \tag{9}$$

The final voltage gain of the proposed converter in CCM operation is given by

$$\frac{V_0}{V_i} = \frac{1+D}{(1-D)^2}. \tag{10}$$

*4) Ampere Second Balance Principle:* Applying the ampere second balance principle on capacitors, the inductors $L_1, L_2, L_3$ can be derived as follows:

$$I_{L1} = \frac{(1+D)V_0}{R(1-D)^2} \tag{11}$$

$$I_{L2} = \frac{(1+D)V_0}{R(1-D)}; I_{L3} = \frac{V_0}{R}. \tag{12}$$

*5) Current Ripple of Inductors:* Inductor current ripple is expressed as,

$$\Delta \mathrm{I}_{L1} = \frac{V_i D}{L_1 f_s}; \Delta \mathrm{I}_{L2} = \frac{V_i D}{(1-D)L_2 f_s} \tag{13}$$

$$\Delta \mathrm{I}_{L3} = \frac{V_i D}{(1-D)L_3 f_s} \tag{14}$$

*6) Voltage Ripple of Capacitors:* Capacitor voltage ripple is expressed as

$$\Delta V_{C_1} = \frac{V_0 D(2-D)}{2(1-D)^2 R f_s C_1}; \Delta \mathrm{V}_{C_2} = \frac{V_0(3-4D)}{2R f_s C_2} \tag{15}$$

$$\Delta \mathrm{V}_{C_3} = \frac{V_0 D}{2(1-D)R f_s C_3}; \Delta \mathrm{V}_{C_4} = \frac{V_0 D}{R f_s C_4}. \tag{16}$$

*7) Voltage Stress and Current Stress:* The voltage stress ($D_1$ and $D_3$) and current stress ($D_2$) of diodes and switch ($M_1$) are obtained through mode-I as follows:

$$V_{D1} = \frac{V_i}{(1-D)}; V_{D3} = V_{D4} = \frac{V_i}{(1-D)^2} \tag{17}$$

$$i_{D2} = \frac{(1+D)i_0}{(1-D)}; i_{M1} = \frac{D(3-D)i_0}{(1-D)^2}. \tag{18}$$

The voltage stress of the diode ($D_2$) and switch ($M_1$) and the current stress of the diodes ($D_1, D_3, D_4$) are obtained through mode-II as follows:

$$V_{D2} = \frac{DV_i}{(1-D)^2}; V_{M1} = \frac{V_i}{(1-D)^2} \tag{19}$$

$$i_{D1} = \frac{(1+D)i_0}{(1-D)}; i_{D3} = i_{D4} = i_0. \tag{20}$$

### B. Discontinuous Conduction Mode

*1) DCM Mode-I:* In this mode of operation, the switch $M_1$ is turned ON for time $(0 \le t \le t_1)$. During this mode, the inductor's current start from zero and increases to peak current at time $t_1$, as shown in Fig. 3(a). The current flow in mode-I of DCM remains the same as mode-I in CCM

$$I_{L3} = \frac{DT_s(V_{C3} - V_{C2})}{L_3}. \tag{21}$$

*2) DCM Mode-II:* In this mode of operation, the switch $M_1$ is turned OFF for time $(t_1 \le t \le t_2)$. During this mode, inductor current decreases from peak current to zero at time $D_{m2}$, as shown in Fig. 3(a). The current flow in mode-II of DCM remains the same as mode-II in CCM. The magnitude of the inductor current in this mode is expressed as

$$I_{L3} = \frac{2V_0}{RD_{m2}}. \tag{22}$$

*3) DCM Mode-III:* In this mode of operation, the switch S is turned OFF for time $(t_2 \le t \le T_s)$. Since the inductors are completely discharged, the input source combined with capacitor $C_4$ provides power to load. The current flow path of mode-III in DCM is shown in Fig. 3(b). The $D_{m2}$ can be calculated as

$$D_{m2} = \frac{2L_{eq} f_s V_0}{RDV_{C1}} \tag{23}$$

$$G_{\mathrm{DCM}} = \frac{V_0}{V_i} = \frac{D + D_{m2}(2D + D_{m2})}{D_{m2}^2}. \tag{24}$$

The normalized time constant ($K_L$) is considered as follows:

$$K_L = \frac{2L_{eq} f_S}{R}. \tag{25}$$

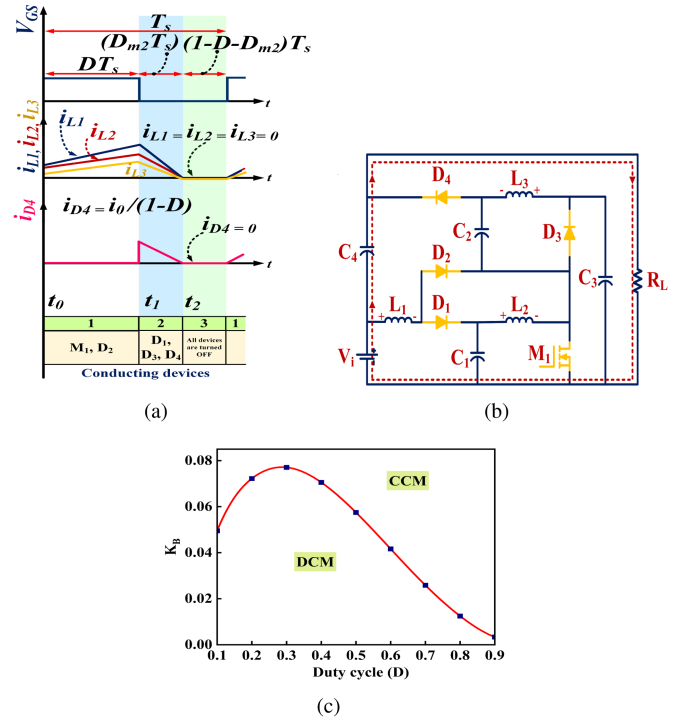



Fig. 3. Proposed converter. (a) DCM theoretical waveform. (b) Mode-III. (c) $K_B$ versus duty cycle (D).

### C. Boundary Conduction Mode

At the boundary, the voltage gain of the proposed converter under CCM equals DCM. The boundary normalized inductor time constant $K_B$ for the inductors is calculated as follows:

$$K_B = D(1-D)\left[\frac{(2D-D^2-1)-\sqrt{D^3-D^2-D+1}}{(D-3)(D+1)}\right]. \tag{26}$$

Fig. 3(c) illustrates the plot between boundary normalized inductor time constant $(K_B)$ and duty cycle (D) where the CCM and DCM regions are indicated. If $K_L > K_B$, the proposed converter is operated at the CCM region or else in the DCM region.

## III. Nonideality Voltage Gain by Considering the Effect of Parasitic Elements of the Proposed Converter With Efficiency Analysis

The equivalent circuit of the proposed converter considering the parasitic elements is shown in Fig. 4(a). The voltage gain of the proposed converter can be identified using the inductor $L_3$.The voltage of the inductor $L_3$ across two modes of operation under CCM is as follows:

Mode 1:

$$V_{L3} = V_{C3} - V_{C2} - i_{L3}\left(R_{C2}+R_{C3}+R_{C2}\right) - i_S R_S. \tag{27}$$

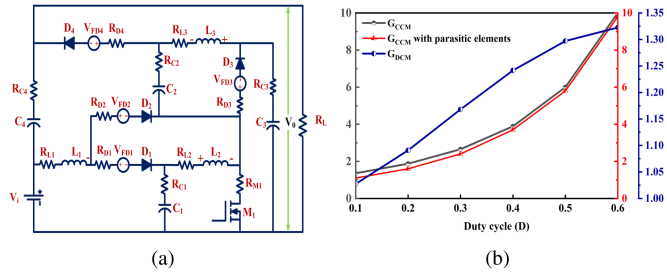



Fig. 4. Effect of parasitic element: (a) Equivalent circuit. (b) Comparison of voltage gain with and without parasitic elements and DCM.

Mode 2:

$$\begin{aligned} V_{L3} &= V_i - i_{L1}(R_{L1}+R_{D1}) - (V_{L1}+V_{L2}) \\ &-(V_{F1}+V_{F3}+V_{F4}) - i_{L2}(R_{L2}+R_{D3}) \\ &-i_{L3}(R_{L3}+R_{D4}) - i_{C2}R_{D4} - V_0. \end{aligned} \tag{28}$$

The voltage gain of the proposed converter considering the parasitic elements is derived as follows:

$$\begin{aligned} V_0 &= V_i\left[\frac{1+D}{(1-D)^2}\right] - i_{C2}(R_{D3}+R_{D4}) + i_{C3}R_{C3} \\ &-V_{F4} - \frac{i_{L3}(R_{C3}+R_{C2})D - R_{L3} + R_{D4}(1-D) - i_S R_s D}{(1-D)} \end{aligned} \tag{29}$$

where $R_{L1}$, $R_{L2}$, and $R_{L3}$ are the internal resistance of the inductors $L_1$, $L_2$, and $L_3$, respectively. $R_{C1}$, $R_{C2}$, $R_{C3}$, and $R_{C4}$ are the equivalent resistance of the capacitors $C_1$, $C_2$, $C_3$, and $C_4$, respectively. $V_{FD1}, V_{FD2}, V_{FD3}, V_{FD4}$, and $R_{D1}, R_{D2}, R_{D3}$, and $R_{D4}$ are the knee voltage and internal resistance of the diodes $D_1$, $D_2$, $D_3$, and $D_4$, respectively. Fig. 4(b) shows the voltage gain versus duty cycle of CCM, CCM with parasitic elements, and DCM. The total power loss of the proposed converter is calculated as follows:

$$\mathrm{P_{loss}} = \mathrm{P_{switch}} + \mathrm{P_{ind.}} + \mathrm{P_{cap.}} + \mathrm{P_{diode}} \tag{30}$$

where the power loss of the switch consists of three components such as conduction loss ($P_{Rds}$), and switching loss ($P_{\mathrm{sw}}$), and coss loss ($P_{\mathrm{coss}}$)

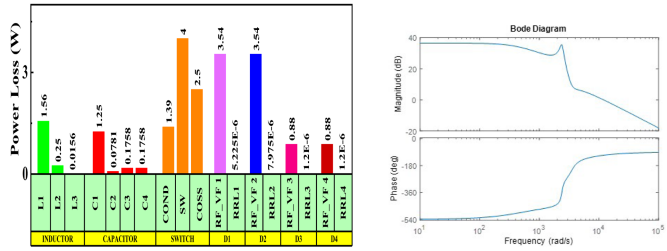
$$\mathrm{P}_{Rds} = \mathrm{R_{ds}D}\left[\frac{(3-\mathrm{D})\mathrm{i_0}}{(1-\mathrm{D})^2}\right]^2; \mathrm{P_{sw}} = \frac{1}{2}\mathrm{V_m I_m f_s(t_{on}+t_{off})} \tag{31}$$

$$\mathrm{P_{Coss}} = \frac{1}{2}\mathrm{V_{M1}^2 f_s C_{oss}} \tag{32}$$

where $R_{ds}$ is the effective resistance between the drain and the source during the ON state of the switch, $f_s$ is the switching frequency, $C_{\mathrm{oss}}$ is the effective capacitance of MOSFET, and $V_{M1}$ is the voltage stress of the switch. $V_m$ and $I_m$ are the maximum voltage and current of $M_1$. $t_{\mathrm{on}}$ and $t_{\mathrm{off}}$ are the turn-ON time and turn-OFF time.

The power loss of the inductors is calculated as follows:

$$\begin{aligned} P_{\mathrm{ind}} &= \left[r_{L1}.\left(\frac{(1+D)V_0}{R(1-D)^2}\right)^2\right] + \\ &\left[r_{L2}.\left(\frac{(1+D)V_0}{R(1-D)}\right)^2\right] + \left[r_{L3}.\left(\frac{V_0}{R}\right)^2\right] \end{aligned} \tag{33}$$




(a) (b)

Fig. 5. (a) Power loss distribution. (b) Bode plot.

where $r_{L1}$, $r_{L2}$, and $r_{L3}$ are the equivalent series resistance of the inductors.

The power loss of the capacitors is calculated as follows:

$$P_{\text{cap}} = \left[r_{C1}.\left(\frac{(1+D)V_0}{R(1-D)}\right)^2\right] + \left[r_{C2}.\left(\frac{V_0}{R}\right)^2\right] + \left[(r_{C3}+r_{C4}).\left(\frac{V_0 D}{(1+D)R}\right)^2\right] \tag{34}$$

where $r_{C1}, r_{C2}, r_{C3}$, and $r_{C4}$ are the equivalent series resistance of the capacitors.

The power loss of the diodes is the combination of forward resistance loss, forward voltage loss, and reverse recovery loss

$$P_{\text{diode}} = P_{\text{FRD}} + P_{\text{VFD}} + P_{\text{RRD}} \tag{35}$$

where, the reverse recovery loss $P_{\text{RRD}}$ is calculated as follows:

$$P_{\text{RRD}} = \sum_{n=1}^{4} V_{(\text{RRM},n)} I_{(\text{RRM},n)} f_s t_b \tag{36}$$

where $V_{\text{RMM},n}$ and $I_{\text{RMM},n}$ are the peak reverse voltage and reverse current of the diodes, respectively. The forward resistance loss $P_{\text{FRD}}$ of the diodes is calculated as follows:

$$P_{\text{FRD}} = \left[r_{\text{FD1}}.\left(\frac{(1+D)I_0}{\sqrt{(1-D)}(1-D)}\right)^2\right] + \left[r_{\text{FD2}}.\left(\frac{(1+D)I_0}{\sqrt{D}(1-D)}\right)^2\right] + \left[(r_{\text{FD3}}+r_{\text{FD4}}).\left(\frac{I_0}{\sqrt{(1-D)}}\right)^2\right]. \tag{37}$$

The forward voltage loss $P_{\text{VFD}}$ of the diodes is calculated as follows:

$$P_{\text{VFD}} = \left[(V_{\text{FD1}}+V_{\text{FD2}}).\left(\frac{(1+D)I_0}{(1-D)}\right)\right] + \left[(V_{\text{FD3}}+V_{\text{FD4}}).(I_0)\right] \tag{38}$$

where $r_{\text{FD},1,2,3,4}$ are the forward resistance of the diodes, $V_{\text{FD},1,2,3,4}$ are the knee voltage of the diodes. Using the above equations, the power loss of the proposed converter can be calculated. Fig. 5(a) shows the power loss distribution of the individual components for the proposed converter topology. The efficiency of the proposed converter is 90.3%, and it is worth mentioning that all components in power losses, such as output capacitor loss of the MOSFET (Coss) loss, switching loss, and conduction loss of the switch, forward resistance loss, forward voltage loss, and reverse recovery loss of diodes, inductor loss, and capacitor loss are considered to obtain the efficiency.

## IV. State Space Model

To derive the state equations, the state variables $x_1$, $x_2$, and $x_3$ are assigned to the inductor currents $L_1$, $L_2$, and $L_3$, respectively. The states $x_4$–$x_7$ are assigned to the capacitor voltages $V_{C1}, V_{C2}, V_{C3}$, and $V_{C4}$. The generic form of the state-space model is represented as

$$\dot{x}(t) = A(D)x(t) + B(D)u(t) \tag{39}$$

where $A(D) = DA_1 + (1-D)A_2$, $B(D) = DB_1 + (1-D)B_2$, and $D \in [0,1]$. The state equations when the switch $M_1$ is turned ON and OFF are shown in (40) and (41) shown at the bottom of the next page, respectively. The state equations for the two modes are combined using the state-space averaging technique as shown in (42) shown at the bottom of the next page. For the state-space averaged model noted in (42), each state variable is assigned a separate variable from $\dot{x_1}$ to $\dot{x_7}$.

The values of the inductors $L_1$ and $L_2 = L_3$ are 0.768 and 1.9 mH, respectively. The values of the capacitors $C_1$, $C_2$, $C_3$, and $C_4$ are 79.68 , 44.53, 25.78, and 4.6875 $\mu F$, respectively. The duty ratio and load resistance (R) values are 0.6 and 128 Ω, respectively. The stability of the proposed topology is inferred from the state space matrix bode plot as shown in Fig. 5(b). The proposed converter's gain margin and phase margin are derived as 0.4372 and 68.6719, respectively. The proposed topology is stable from the parameters inferred from the bode plot as shown in Fig. 5(b)

*Remark 1:* This statement highlights that the evolution of the system state of a dc–dc converter is determined by both the continuous dynamics of the system and the status of the switch, which is represented by the variable $\sigma$. The switch can either be ON $(D = 1)$ or OFF $(D = 0)$, which affects the behavior of the converter. The statement also mentions that while similar models have been used for the simulation and control design of dc–dc converters, the use of switched models for SDC is not very common. This implies that there is a need for more research and development in the area of SDC based on switched models for dc–dc converters.

The switching law is as same as that of the general system (39). It is described by

$$\dot{x}(t) = A_{\varpi(t)}x(t) + B_{\varpi(t)}u(t) \tag{43}$$

where $x(t) \in \mathbb{R}^n$ is the state, $u(t)$ represent the control input, and $\varpi(t) : [0,\infty) \to \mathcal{I} = 1, 2, \ldots, n$ is the switching signal. The $i$th subsystem is activated when $\varpi(t) = i$. Let $t_f^{\varpi}$ be the switching instant satisfying $t_1^{\varpi} < t_2^{\varpi} < \cdots < t_f^{\varpi}$.

## V. Controller Design

The sampling instants are denoted as $0 = t_0 < t_1 < \cdots < t_k < \cdots$. The following SD controllers with zero-order hold (ZOH) are designed:

$$u(t) = K_{\varpi(t_k)}x(t_k) \tag{44}$$

where $K_{\varpi(t)}$ is the controller gain to be designed. Set the sampling interval $h_k = t_{k+1} - t_k$ and satisfy $0 \le h_k \le h_{\text{Max}}$, for all $k \ge 0$. Then, by substituting (44) into (43), one gets

$$\dot{x}(t) = A_i x(t) + B_i K_i x(t_k). \tag{45}$$

When contemplating asynchronous switching, the time of the switch is denoted as $t_k + \tilde{t}$, where $\tilde{t}$ is a value within the range of $(0, h_{\text{Max}}]$. Prior to the switch when $t$ belongs to the interval $[t_k, t_k + \tilde{t})$ and $\varpi(t)$ equals $i$, there is a match between the system and controller. However, following the switch, when $t$ belongs to the interval $[t_k + \tilde{t}, t_{k+1})$ and $\varpi(t$ equals $j$, the controller remains unchanged as it has not yet received the sampling signal. As a result, there is a mismatch between the system and the controller. This circumstance can be determined by analysis

$$\dot{x}(t) = \begin{cases} A_i x(t) + B_i K_i x(t_k), \ t \in [t_k, t + \tilde{t}) \\ A_j x(t) + B_j K_i x(t_k), \ t \in [t + \tilde{t}, t_{k+1}). \end{cases} \tag{46}$$

The following definitions are necessary to attain this goal.

*Definition 1:* Ref. [27] The relation (45) is considered exponentially stable when there exist positive values of $\alpha$ and $\beta$, then the subsequent condition is satisfied

$$\|x(t)\| \le \beta e^{-\alpha(t-t_0)} \|x(t_0)\|_c \quad \forall t \ge t_0 \tag{47}$$

where $\alpha$ and $x(t_0)$ represent the exponential delay rate and initial value, respectively, at $t = t_0$.

*Definition 2:* Ref. [27] Assuming a constant $\tau_d > 0$, it can be guaranteed that the time interval between two consecutive switches is at least $\tau_d$, i.e., $t^{\sigma}_{s+1} - t^{\sigma}_{s} > \tau_d$. If there exists $N_0 > 1$ such that

$$N_\sigma(T, t) \le N_0 + \frac{T - t}{\tau_d} \quad \forall T > t \ge t_0 \tag{48}$$

where $N_\sigma(t, T)$ denotes the number of changes to $(t, T)$.

## VI. Stability and Stabilization Analysis

This section will cover the examination of stability analysis and controller design. The ADT switching mechanism will be employed, and Theorem 1 will provide an exponential stability criterion for system (45) based on specific sampling interval conditions. For simplicity, it is denoted as

$$\chi^T(t) = [x^T(t)\ \dot{x}^T(t)\ x^T(t_k)]$$
$$e_l = [0_{n\times(l-1)n}\ I_n\ 0_{n\times(3-1)n}]^T.$$

*Theorem 1:* For known gain matrices $K_i$, and positive scalars $\delta, \gamma, \sigma_1, \sigma_2$, and $h_{\text{Max}} > 0$, the system (45) is exponentially stable if there exist matrices $P_i > 0, P_{ij} > 0, Q_i > 0, Q_{ij} > 0, i \ne j \in \mathcal{I}$, any matrices $\mathcal{U}_i$, and the subsequent LMIs satisfied

$$\Xi_i < 0 \tag{49}$$

$$\Xi_{ij} < 0 \tag{50}$$

$$P_{ij} < P_i, P_j < \tilde{\mu} P_{ij}, Q_{ij} < \tilde{\mu} Q_i \tag{51}$$

where

$$\Xi_i = 2e_1^T P_i e_2 + \delta e_1^T P_i e_1 - e_1^T Q_i e_1 + e_1^T Q_i e_3 - e_3^T Q_i e_3 + 2h_{\text{Max}} e_1^T Q_i e_2 - 2h_{\text{Max}} e_3^T Q_i e_2$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{dV_{C1}}{dt} \\ \frac{dV_{C2}}{dt} \\ \frac{dV_{C3}}{dt} \\ \frac{dV_{C4}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_3} & \frac{1}{L_3} & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{RC_4} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix} + V_i \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{1}{RC_4} \end{bmatrix} \tag{40}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{dV_{C1}}{dt} \\ \frac{dV_{C2}}{dt} \\ \frac{dV_{C3}}{dt} \\ \frac{dV_{C4}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} & \frac{1}{L_3} \\ \frac{1}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & \frac{-1}{C_3} & 0 & 0 & 0 & 0 \\ \frac{1}{C_4} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix} + V_i \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ \frac{1}{L_3} \\ 0 \\ 0 \\ 0 \\ \frac{-1}{RC_4} \end{bmatrix} \tag{41}$$

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \\ \dot{x_4} \\ \dot{x_5} \\ \dot{x_6} \\ \dot{x_7} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-D)}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & \frac{-(1-D)}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{-D}{L_3} & \frac{(2D-1)}{L_3} & \frac{(1-D)}{L_3} \\ \frac{(1-D)}{C_1} & \frac{(2D-1)}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{(2D-1)}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{(1-D)}{C_3} & \frac{-1}{C_3} & 0 & 0 & 0 & 0 \\ \frac{(1-D)}{C_4} & 0 & 0 & 0 & 0 & 0 & \frac{D}{RC_4} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ \frac{(1-D)}{L_3} \\ 0 \\ 0 \\ 0 \\ \frac{2D-1}{RC_4} \end{bmatrix} V_i. \tag{42}$$

$$
\begin{aligned}
&+ \delta h_{\text{Max}} e_1^T Q_i e_1 - \delta h_{\text{Max}} e_1^T Q_i e_3 + \delta h_{\text{Max}} e_3^T Q_i e_3 \\
&- 2e_2^T \sigma_1 \mathcal{U}_i e_2 + 2e_2^T \sigma_1 \mathcal{U}_i A_i e_1 + 2e_2^T \sigma_1 \mathcal{U}_i B_i K_i e_3 \\
&- 2e_1^T \sigma_2 \mathcal{U}_i e_2 + 2e_1^T \sigma_2 \mathcal{U}_i A_i e_1 + 2e_1^T \sigma_2 \mathcal{U}_i B_i K_i e_3, \\
\Xi_{ij} = {} & 2e_1^T P_{ij} e_2 + \delta e_1^T P_{ij} e_1 - e_1^T Q_{ij} e_1 + e_1^T Q_{ij} e_3 \\
&- e_3^T Q_{ij} e_3 + 2h_{\text{Max}} e_1^T Q_{ij} e_2 - 2h_{\text{Max}} e_3^T Q_{ij} e_2 \\
&+ \delta h_{\text{Max}} e_1^T Q_{ij} e_1 - \delta h_{\text{Max}} e_1^T Q_{ij} e_3 + \delta h_{\text{Max}} e_3^T Q_{ij} e_3 \\
&- 2e_2^T \sigma_1 \mathcal{U}_{ij} e_2 + 2e_2^T \sigma_1 \mathcal{U}_{ij} A_j e_1 + 2e_2^T \sigma_1 \mathcal{U}_{ij} B_j K_i e_3 \\
&- 2e_1^T \sigma_2 \mathcal{U}_{ij} e_2 + 2e_1^T \sigma_2 \mathcal{U}_{ij} A_j e_1 + 2e_1^T \sigma_2 \mathcal{U}_{ij} B_j K_i e_3.
\end{aligned}
$$

Then, the ADT satisfies

$$\tilde{\lambda}_a \geq (1 + \frac{\delta h_{\text{Max}} + ln\tilde{\mu}}{\gamma h_{\text{Max}}}) h_{\text{Max}}. \tag{52}$$

*Proof 1:* There are two possible outcomes for sample intervals when considering a switching system (45): 1) no switch occurs at all during the sampling interval; and 2) one switch occurs during the sampling interval.

Case A: Sampling interval with no switch. When the $i$th subsystem is turned on, which occurs across the entire interval $[t_k, t_{k+1})$. From (46), The dynamic of the closed-loop system is represented by

$$\dot{x}(t) = A_i x(t) + B_i K_i x(t_k). \tag{53}$$

Consider the following LF candidate:

$$
\begin{aligned}
V_i(t) = {} & x^T(t) P_i x(t) + (t_{k+1} - t)[x^T(t) - x^T(t_k)] \\
& \times Q_i [x(t) - x(t_k)], \ t \in [t_k, t_{k+1}).
\end{aligned} \tag{54}
$$

Taking the derivative of $V_i(t)$

$$
\begin{aligned}
\dot{V}_i(t) \leq {} & -\delta V_i(t) + 2x^T(t) P_i \dot{x}(t) + \delta x^T(t) P_i x(t) \\
& - [x^T(t) - x^T(t_k)] Q_i [x(t) - x(t_k)] \\
& + 2h_{\text{Max}} [x^T(t) - x^T(t_k)] Q_i \dot{x}(t) \\
& + \delta h_{\text{Max}} [x^T(t) - x^T(t_k)] Q_i [x(t) - x(t_k)].
\end{aligned} \tag{55}
$$

For any dimensional free weighting matrices $\mathcal{U}_i$ with scalars $\sigma_1, \sigma_2$, the resulting equation satisfies

$$0 = 2[\dot{x}^T(t)\sigma_1 + x^T(t)\sigma_2] \mathcal{U}_i [-\dot{x}(t) + A_i x(t) + B_i K_i x(t_k)]. \tag{56}$$

With derivative of the LF (54), it can be concluded that for $t \in [t_k, t_{k+1})$

$$\dot{V}_i(t) + \delta V_i(t) \leq \chi^T(t) \Xi_i \chi(t) \tag{57}$$

where $\Xi_i$ is defined in Theorem 1. If $\Xi_i < 0$, the considered system is stable, this implies that

$$\dot{V}_i(t) \leq -\delta V_i(t) \quad \forall t \in [t_k, t_{k+1}). \tag{58}$$

Integrating the above (58)

$$\dot{V}_i(t_{k+1}) \leq e^{-\delta(t_{k+1} - t_k)} V_i(t_k) \quad \forall t \in [t_k, t_{k+1}). \tag{59}$$

Case B: The sampling interval with one switch

In this particular scenario, the interval $[t_k, t_{k+1})$ will play host to not one but two distinct subsystems, specifically $\varpi(t_k)$ and $\varpi(t_{k+1}) - j \neq i$. Only when the sample is taken so can the controller obtain information about the switching in the system. Based on (46), the $i$th subsystem will be active accordingly if $t \in [t_k, t_k + \tilde{t}]$. Along the same lines as Case A, one can conclude that

$$\dot{V}_i(t) \leq e^{-\delta(t - t_k)} V_i(t_k). \tag{60}$$

When $t \in (t_k + \tilde{t}, t_{k+1})$, yields

$$\dot{x}(t) = A_j x(t) + B_j K_i x(t_k). \tag{61}$$

Consider the following LF for (61):

$$
\begin{aligned}
V_{ij}(t) = {} & x^T(t) P_{ij} x(t) + (t_{k+1} - t)[x^T(t) - x^T(t_k)] \\
& \times Q_{ij} [x(t) - x(t_k)].
\end{aligned} \tag{62}
$$

Similar to the process in Case A and from the LMI conditions (49) and (50), yields

$$\dot{V}_{ij}(t) - \gamma V_{ij}(t) < 0. \tag{63}$$

Integrating (63)

$$V_{ij}(t) < e^{\gamma(t - t_k - \tilde{t})} V_{ij}(t_k + \tilde{t}). \tag{64}$$

From the LF (51), (54), and (62)

$$V_{ij}(t_k + \tilde{t}) \leq \tilde{\mu} V_i((t_k + \tilde{t})^-) \tag{65}$$

$$V_j(t_{k+1}) \leq \tilde{\mu} V_{ij}(t_{k+1}^-). \tag{66}$$

In conjunction with (59), (60), and (64)–(66), the connection between $V_{ij}(t_{k+1}^-)$ and $V_i(t_k)$ can be described as

$$
\begin{aligned}
V_{\varphi(t)}(t) & \leq \tilde{\mu} \mathcal{N}_{\varpi}(t_0, t) e^{(\delta+\gamma)\mathcal{N}_{\varpi}(t_0, t) h_{\text{Max}}} e^{-\delta(t - t_0)} V_{\varpi(t_0)}(t_0) \\
& \leq e^{((\delta+\gamma)h_{\text{Max}} + ln\tilde{\mu})(\mathcal{N}_0 + \frac{t - t_0}{\tilde{\lambda}_a})} V_{\varpi(t_0)}(t_0) \\
& \leq e^{((\delta+\gamma)h_{\text{Max}} + ln\tilde{\mu})\mathcal{N}_0} e^{(\frac{(\delta+\gamma)h_{\text{Max}} + ln\tilde{\mu}}{\tilde{\lambda}_a} - \delta)(t - t_0)} V_{\varpi(t_0)}(t_0).
\end{aligned} \tag{67}
$$

Defining $\rho = e^{((\delta+\gamma)h_{\text{Max}} + ln\tilde{\mu})(\mathcal{N}_0)}$, $\eta = (\delta - \frac{(\delta+\gamma)h_{\text{Max}} + ln\tilde{\mu}}{\tilde{\lambda}_a}) > 0$, the ADT $\tilde{\lambda}_a$ prescribed in (52), then

$$V_{\varphi(t)}(t) < \rho e^{-\lambda(t - t_0)} V_{\varphi(t_0)}(t_0) \tag{68}$$

Therefore, from the LF, there exists the scalars $\bar{a}$ and $\bar{b}$

$$
\begin{aligned}
\bar{a} ||x(t)||^2 & \leq V_{\varphi(t)}(t) \\
V_{\varphi(t)}(t_0) & \leq \bar{b} ||x(t_0)||_{\rho}^2.
\end{aligned} \tag{69}
$$

Therefore

$$||x(t)|| \leq \rho \sqrt{\frac{\bar{b}}{\bar{a}}} e^{-\lambda(t - t_0)} ||x(t_0)||_{\rho}. \tag{70}$$

It is possible to conclude, in accordance with Definitions 1 and 2, that the system (45) is exponentially stable whenever a switching signal satisfies the ADT (52). The proof is completed. ■

## VII. Sampled-Data Controller Layout

Based on the preceding study, this section analyzes the controller design for the system (45).

*Theorem 2:* For known positive scalars $\delta, \gamma, \sigma_1, \sigma_2, h_{\text{Max}} > 0$, the system (45) is exponentially stable, if there exist matrices $P_i > 0, P_{ij} > 0, Q_i > 0, Q_{ij} > 0$, any matrices $\mathcal{U}_i, Y_i$, nonsingular matrices $\Theta_i, i \neq j \in \mathcal{I}$, and the subsequent inequalities are satisfied

$$\bar{\Xi}_i < 0 \tag{71}$$

$$\bar{\Xi}_{ij} < 0 \tag{72}$$

$$\bar{P}_{ij} < \bar{P}_i, \bar{P}_j < \tilde{\mu}\bar{P}_{ij}, \bar{Q}_{ij} < \tilde{\mu}\bar{Q}_i \tag{73}$$

where

$$\begin{aligned}\bar{\Xi}_i = {} & 2e_1^T\bar{P}_ie_2 + \delta e_1^T\bar{P}_ie_1 - e_1^T\bar{Q}_ie_1 + e_1^T\bar{Q}_ie_3 \\ & - e_3^T\bar{Q}_ie_3 + 2h_{\text{Max}}e_1^T\bar{Q}_ie_2 - 2h_{\text{Max}}e_3^T\bar{Q}_ie_2 \\ & + \delta h_{\text{Max}}e_1^T\bar{Q}_ie_1 - \delta h_{\text{Max}}e_1^T\bar{Q}_ie_3 + \delta h_{\text{Max}}e_3^T\bar{Q}_ie_3 \\ & - 2e_2^T\sigma_1\tilde{\mathcal{U}}_ie_2 + 2e_2^T\sigma_1A_i\Theta_ie_1 + 2e_2^T\sigma_1B_iY_ie_3 \\ & - 2e_1^T\sigma_2\Theta_ie_2 + 2e_1^T\sigma_2A_i\Theta_ie_1 + 2e_1^T\sigma_2B_iY_ie_3 \\ \bar{\Xi}_{ij} = {} & 2e_1^TP_ie_2 + \delta e_1^TP_ie_1 - e_1^TQ_ie_1 + e_1^TQ_ie_3 \\ & - e_3^TQ_ie_3 + 2h_{\text{Max}}e_1^TQ_ie_2 - 2h_{\text{Max}}e_3^TQ_ie_2 \\ & + \delta h_{\text{Max}}e_1^TQ_ie_1 - \delta h_{\text{Max}}e_1^TQ_ie_3 + \delta h_{\text{Max}}e_3^TQ_ie_3 \\ & - 2e_2^T\sigma_1\Theta_ie_2 + 2e_2^T\sigma_1A_j\Theta_ie_1 + 2e_2^T\sigma_1B_jY_ie_3 \\ & - 2e_1^T\sigma_2\Theta_ie_2 + 2e_1^T\sigma_2A_j\Theta_ie_1 + 2e_1^T\sigma_2B_jY_ie_3.\end{aligned}$$

Then, the ADT satisfies the $\tilde{\lambda}_a \geq (1 + \frac{ln\tilde{\mu}}{\gamma})$ and the controller gain is given by $K_i = Y_i\Theta_i^{-1}$.

*Proof 2:* First, it is defined that $\bar{P}_i = \Theta_iP_i\Theta_i$, $\bar{P}_{ij} = \Theta_iP_{ij}\Theta_i$, $\bar{Q}_i = \Theta_iQ_i\Theta_i$, $\bar{Q}_{ij} = \Theta_iQ_{ij}\Theta_i$, $\mathcal{U}_i = \Theta_i^{-1}$, $\mathcal{U}_{ij} = \Theta_i^{-1}$. In addition, conditions (71)–(73) are derived from premultiplying and postmultiplying (49)–(51) by $\Theta_i$, respectively, which completes the proof. ■

## VIII. Comparison With Recently Developed Nonisolated Converter Topologies

This section compares the proposed converter with the recently developed nonisolated-based quadratic and nonquadratic converters in terms of voltage gain ($G_{\text{CCM}}$), normalized voltage and current stress of the switch, the ratio of switch voltage stress to the voltage gain ($V_{\text{SW}}/G_{\text{CCM}}$), and ratio of voltage gain to TCC ($G_{\text{CCM}}$/ TCC). Fig. 6(a) shows the comparison of voltage gain versus duty cycle of the proposed converter with various QBC found in the literature [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], and [17]. It is evident that the proposed converter has higher voltage gain as compared with other quadratic-based boost converters found in literature [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], and [17]. Fig. 6(b) compares the proposed converter normalized voltage stress of the switch with the other recently developed QBCs. From Fig. 6(b), it is noted that the proposed converter

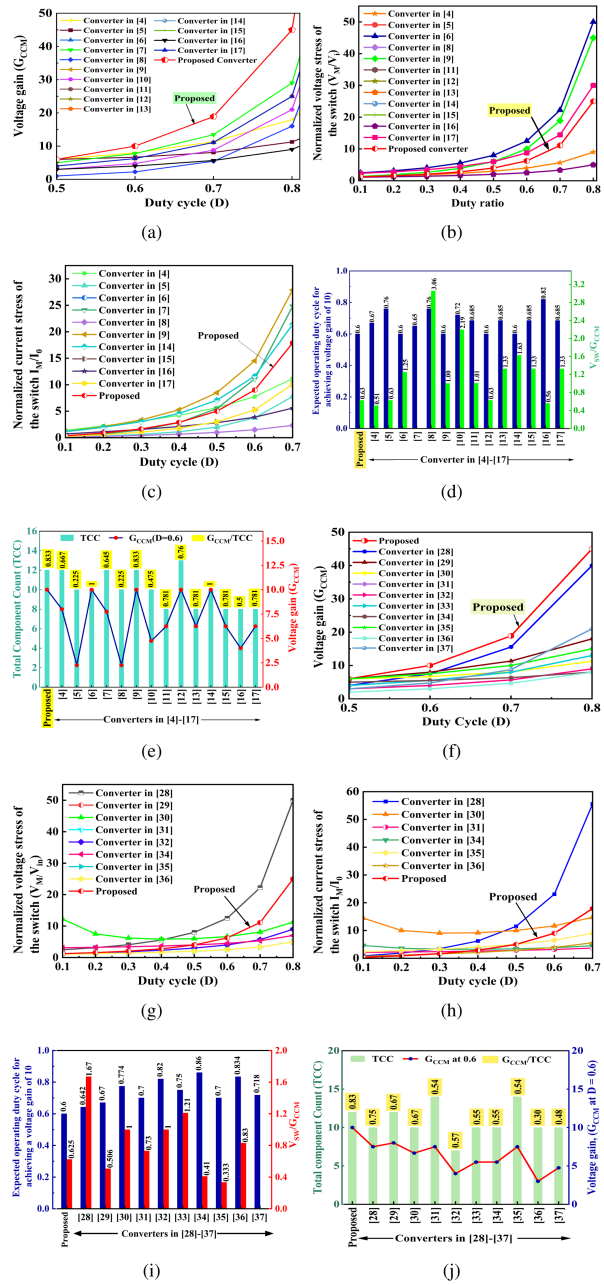



Fig. 6. Comparison of the proposed converter with recently developed quadratic converters. (a) $G_{\text{CCM}}$ versus duty ratio. (b) Normalized voltage stress of the switch. (c) Normalized current stress of the switch. (d) Expected operating duty cycle to achieve a voltage gain of 10 and $V_{\text{SW}}$ / $G_{\text{CCM}}$. (e) $G_{\text{CCM}}$/TCC; Comparison of the proposed converter with recently developed nonquadratic converters. (f) $G_{\text{CCM}}$ versus duty ratio. (g) Normalized voltage stress. (h) Normalized current stress. (i) Expected operating duty cycle to achieve a voltage gain of 10 and $V_{\text{SW}}$ /$G_{\text{CCM}}$. (j) $G_{\text{CCM}}$/TCC.

attains lower voltage stress than other recently developed QBCs except for the converter designed in [4] and [16]. Also, the converter in [10], [11], [12], and [13] has the same voltage stress as the proposed converter. Fig. 6(c) shows the normalized current stress of the switch where the normalized current stress of the proposed converter is lower than other recently developed QBCs except in [5], [8], [15], [16], and [17]. It should be noted that the increased duty cycle would provide high voltage

gain and increase the voltage stress and current stress of the semiconductor switch. Therefore, it is important to compare the converters by considering a common voltage gain of 10, which could provide the actual duty cycle required by each converter to attain a required voltage gain of 10. At the same time, the voltage stress of the switch can be evaluated effectually by considering the ratio of voltage stress to the voltage gain of the converter. This ratio could provide the actual voltage stress of the switch with respect to the obtained voltage level.

Fig. 6(d) shows the ratio of voltage stress of the switch ($V_{SW}$) to voltage gain ($G_{CCM}$) for various QBCs found in the literature [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], and [17] with proposed converter. It is noted that the ratio of ($V_{SW}/G_{CCM}$) of the proposed converter is found to be low compared with the converters in [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], and [17]. Although the converters in [4] and [16] have lower voltage stress, it should be noted that the voltage gain of the converter is low as compared with the proposed converter, which is clear from the Fig. 6(a). From Fig. 6(d), it is also noted that the proposed converter is operated at a reduced duty cycle of 0.6 to attain a voltage gain of 10, which is low as compared with the other converter found in the literature [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], and [17]. The increase in the duty cycle would increase the power loss of the individual components of the proposed converter, thereby reducing the performance of the converter. Fig. 6(e) shows the comparison of TCC, and the ratio of voltage gain to TCC ($G_{CCM}$/ TCC). From Fig. 6(e), it is evident that the ratio of $G_{CCM}$/ TCC is high for the proposed converter when compared to the converters found in the literature [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], and [17]. The converters found in [6] and [14] have a high $G_{CCM}$/ TCC ratio of 1, and the voltage gain of those converters is the same as that of the proposed converter. However, the ratio of voltage stress of the switch ($V_{SW}$) to voltage gain ($G_{CCM}$) of the converter is found to be 1.25 and 1.63, respectively, as shown in Fig. 6(e), which is higher than the proposed converter ratio. This increased voltage stress could increase the failure rate of the switch and reduce the reliability of the converter. Also, the converter in [12] has the same voltage gain, but the TCC of the converter is higher than the proposed converter. So, the $G_{CCM}$/ TCC ratio of the developed converter in [12] is lower than the proposed converter.

Fig. 6(f) shows the voltage gain comparison of the proposed converter with recently developed nonquadratic converters in [28], [29], [30], [31], [32], [33], [34], [35], [36], and [37]. From Fig. 6(f), it is evident that the proposed converter has higher voltage gain for various duty cycles as compared with recently developed converters in [28], [29], [30], [31], [32], [33], [34], [35], [36], and [37]. Fig. 6(g) and 6(h) shows the normalized voltage and current stress of the semiconductor switch, respectively. From Fig. 6(g), it is noted that the voltage stress and current stress of the semiconductor switch are lower than the converters [28] and [30]. The converters in [31], [32], and [34] have only 36% less voltage stress than the proposed converter. Fig. 6(i) shows the ratio of voltage stress of the switch ($V_{SW}$) to voltage gain ($G_{CCM}$) across various nonisolated

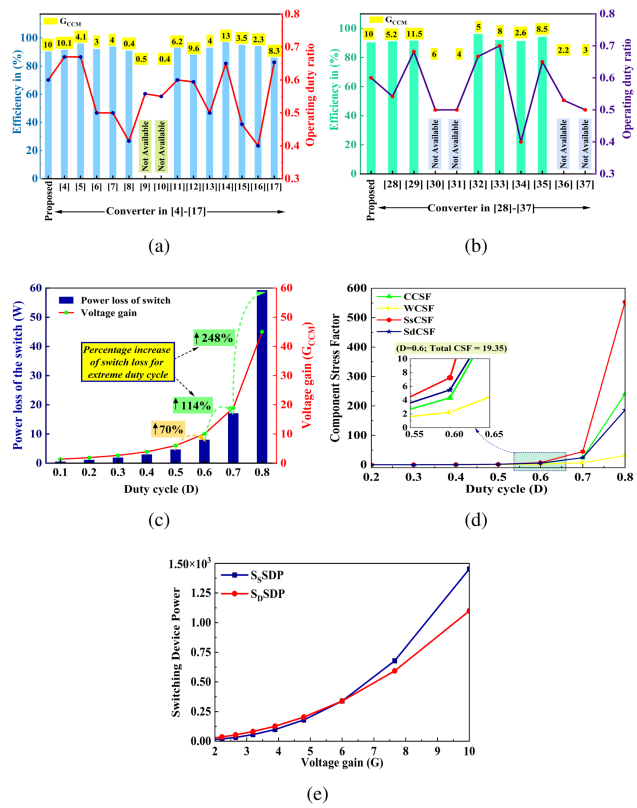



Fig. 7. Comparison of the proposed converter with recently developed converters. (a) Efficiency comparison with operating duty ratio of quadratic converters. (b) Efficiency comparison with operation duty ratio of nonquadratic converters. (c) Power loss of the switch with voltage gain for different duty ratio. (d) CSF. (e) SDP.

converters found in the literature [28], [29], [30], [31], [32], [33], [34], [35], [36], and [37] with the proposed converter. It is noted that the ratio of ($V_{SW}/G_{CCM}$) is lower (i.e., 0.625) than other recently developed converters found in [28], [29], [30], [31], [32], [33], [34], [35], [36], and [37] except the converters in [29], [34], and [35]. However, the converters found in [29], [34], and [35] have been operated at higher duty cycle values, which may increase the power loss of the semiconductor switch. Fig. 6(j) shows the comparison of TCC and the ratio of voltage gain to TCC. It is noted that the proposed converter attains a higher voltage gain of 10 by utilizing only 12 components, and it has a $G_{CCM}$/ TCC ratio of 0.83, which is higher as compared with recently developed converters found in [28], [29], [30], [31], [32], [33], [34], [35], [36], and [37].

Fig. 7(a) and (b) shows the comparison of efficiency, operating duty ratio, and voltage gain of a proposed converter with recently developed QBCs and nonquadratic converters. The efficiency of the proposed converter is 90.3% where multiple components of power losses such as output capacitor loss of the MOSFET (Coss) loss, switching loss, conduction loss of the switch, forward resistance loss, forward voltage loss, and reverse recovery loss of diodes, inductor loss, and capacitor loss are considered to obtain the proposed converter efficiency. At the same time, the other developed converters in [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [28], [29], [30], [31], [32], [33],


Fig. 8. (a) Experimental set-up of the proposed converter. (b) $V_i$ & $V_0$. (c) $I_{in}$ & $I_0$. (d) $I_{L2}$ & $I_{L1}$. (e) $I_{L3}$ voltage across (f) $D_1$ & $D_2$, (g) $D_3$ & $D_0$, (h) $C_1$ & $C_2$, and (i) $C_3$ & $C_4$. (j) Voltage and current across switch $M_1$. (k) $V_0$ and $I_0$ for changing the duty cycle with 128 Ω. (l) $V_0$ and $I_0$ for changing the load values at 60 % duty cycle. (m) $V_0$ and $I_0$ for changing the load values at constant input voltage in closed-loop. (n) $V_0$ for change in input voltages at constant load in closed loop.

[34], [35], [36], and [37] have not included all the components of power loss to evaluate the developed converter efficiency. The duty cycle closer to unity is termed as extreme duty cycle of the converters. At the same time, the value of the extreme duty cycle may vary for each topology depending on the voltage gain value. Fig. 7(c) shows the impact of power loss with respect to the duty cycle of the proposed converter. Fig. 7(c) indicates that the proposed converter can attain a higher voltage gain at the duty cycle of 0.7 and above. It should be noted that the power loss of the switch ($P_{\text{switch}}$) is significantly increased and reduces the efficiency of the proposed converter when it is operated at higher duty cycle values (0.7 and above). From Fig. 7(c), it is observed that the changes in the duty cycle from 0.5 to 0.6 lead to an increase in an additional power loss of the switch by 70%. When the duty cycle changes from 0.6 to 0.7, the power loss of the switch increases by 114%. Also, if the duty cycle varies from 0.7 to 0.8, the power loss of the switch shall increase by 248%. Fig. 7(d) shows the component stress factor (CSF) of the proposed converter for different duty cycles. The CSF is high for extreme duty cycle conditions (i.e., $D \geq 0.7$) [38]. Therefore, it is better to operate the proposed converter at a less-duty cycle (i.e., D = 0.6) with 50 kHz where the total CSF is 19.35. Fig. 7(e) shows the switch device power (SDP) rating for different duty cycles. The SDP rating considers the voltage and current stress of the semiconductor device (switch and diodes) and provides a quantifiable value that indicates the power handling capability of the devices [39]. It is used to estimate the converter's cost and thermal requirements. From the CSF and SDP analysis, it is clear that the proposed converters have higher voltage gain with reduced switching stress that suits well for renewable energy applications.

TABLE I
COMPONENT DETAILS OF EXPERIMENTAL SETUP

| Parameters | Values | Dimension |
|---|---|---|
| $M_1$ | IXFH120N30X3 | 0.62"(L) x 0.19"(B) |
| $L_1$ | 0.7 mH | 1.70"(L) x 1.20"(B) |
| $L_2$, $L_3$ | 1.9 mH | 1.30"(L) x 0.90"(B) |
| $C_1$ | ESY826M063AG4, (82 $\mu$F) | 0.59"(L) x 0.31"(D) |
| $C_2$ | ESY476M100AH9, (47 $\mu$F) | 0.49"(L) x 0.39"(D) |
| $C_3$ | ESK336M160AH4, (33 $\mu$F) | 0.78"(L) x 0.39"(D) |
| $C_4$ | ESK475M200AH1, (4.7 $\mu$F) | 0.47"(L) x 0.39"(D) |
| $D_1$,$D_2$ | MUR1610CTG | 0.38"(L) x 0.16"(B) |
| $D_3$, $D_4$ | MUR1620CTG | 0.38"(L) x 0.16"(B) |

L- Length, B- Breadth, D- Diameter, $L_1$,$L_2$,$L_3$-Inductors, $C_1$,$C_2$,$C_3$,$C_4$-Capacitors, $D_1$,$D_2$,$D_3$,$D_4$-Diodes

## IX. EXPERIMENTAL RESULTS

The proposed converter is designed and examined its operation through a laboratory-based prototype with 200 W and a switching frequency of 50 kHz. The experimental prototype is shown in Fig. 8(a). The cyclone V real-time controller, ACS712 current sensor, and LV20-P voltage sensor are utilized. Table I shows the component details with their dimensions to develop the proposed converter in the laboratory-based prototype. The

power density of the proposed converter is 1.02 kW/L. The operation of the proposed converter is verified through open-loop and closed-loop conditions. Fig. 8(b) and (c) shows the input and output voltage experimental waveforms and input and output current experimental waveforms of the proposed converter in the open-loop condition, where it provides 152 V for an input voltage of 16 V at a 0.6 duty ratio. The input and output currents are 13.6 and 1.19 A, respectively. Fig. 8(d) and (e) shows the inductor current experimental waveform of $L_1$, $L_2$, and $L_3$, where the values are 12.5, 5.2, and 1.29 A, respectively. Fig. 8(f) and (g) shows the diode voltage experimental waveforms of $D_1$, $D_2$, and $D_3$, $D_4$, where the values are 38, 56, and 94, 95 V, respectively. Fig. 8(h) and (i) shows the capacitor voltage experimental waveforms of $C_1$, $C_2$, and $C_3$, $C_4$, where the values are 38.8, 57, and 98, 135 V, respectively. Fig. (j) shows the voltage and current stress waveform of the semiconductor switch, where the values are 94 V and 9.5 A, respectively. The dynamic behavior of the proposed converter is analyzed in open-loop conditions by changing the duty ratio and load values. The duty ratio of the converter is changed from 0.5 to 0.7. The load values are changed from 150 to 250 W. Fig. 8(k) and (l) shows the open-loop output voltage and output current waveforms for changing the duty ratio and load values, respectively. The dynamic behavior of the proposed converter is analyzed in closed-loop conditions by changing the load and input values. Fig. 8(m) shows the output voltage and current waveform for changing the load values in the closed loop condition. Fig. 8(n) shows the output voltage waveform for change in input values in the closed loop condition. For the reference voltage of 152 V, the proposed converter is tested for different input voltages (16, 20, 24 V) for a constant load of 128 Ω. Moreover, according to LMIs in Theorem 2, when $\alpha = 0.1$ and $h_{\text{Max}} = 0.01$, the control gain obtained via the LMI Control toolbox of MATLAB: $K_1 = [-0.4314 \ -0.0930 \ 0.0524 \ -1.0253 \ 0.0023 \ -0.2618 \ -0.0322]$, $K_2 = [-0.0431 \ -0.0093 \ 0.0052 \ -0.1025 \ 0.0002 \ -0.0262 \ -0.0032]$. With the help of the above gain matrices, the experimental results of the closed-loop conditions are obtained. From Fig. 8(m) and (n), it is evident that the closed-loop control method is effectively working during change in the load and input values. Therefore, the sampled-data controller can be implemented for any other converters.

## X. Conclusion

A new nonisolated dc–dc converter has been implemented for higher voltage gain at a lower duty ratio. The operation of the proposed converter has been examined in CCM and DCM. A laboratory-based prototype model has been tested with 200 W. The steady-state and dynamic conditions are tested with open-loop and closed-loop conditions to showcase the effectiveness of the proposed topology. The individual component results have been taken in open-loop steady-state conditions. Changes in duty ratio with constant input voltage and changes in load values with constant duty cycle have been examined in open-loop dynamic conditions. The SDC strategy has been implemented in closed-loop operation to enhance the performance of the converter. The two dynamic conditions have been examined to validate the closed-loop controller performance of the proposed converter. Changes in the input values with the constant load and changes in the load values with the constant input voltage have been tested in closed-loop conditions. The power density of the proposed converter is 1.02 kW/L. Experimental results have been matched with the theoretical results. The proposed converter can be extendable by incorporating the different VMCs that are available in the existing literature or by extending the presented VMC with multiple times, depending on the required voltage level. Also, future work on the proposed converter could be extended by incorporating reliability analysis to predict the failure rate of each component of the proposed converter.

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